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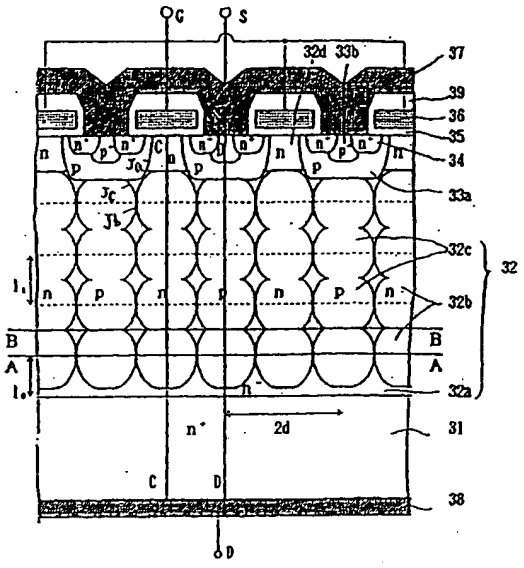
(54) Semiconductor device with alternating conductivity type layer and method of manufacturing the same

(57) The semiconductor device according to the invention includes a semiconductive substrate region 32, through that a current flows in the ON-state of the device and that is depleted in the OFF-state. The semiconductive substrate region 32 includes a plurality of vertical alignments of n-type buried regions 32b and a plurality of vertical alignments of p-type buried regions 32c. The vertically aligned n-type buried regions 32b and the vertically aligned p-type buried regions 32c are alternately arranged horizontally.

The n-type buried regions 32b and p-type buried regions 32c are formed by diffusing respective impurities into highly resistive n--type layers 32a laminated one by one epitaxially.

Fig.1



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Description

[0001] The present invention relates to a vertical semiconductor structure that facilitates realizing a high breakdown voltage and a high current capacity together in the insulated gate field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), bipolar transistors, diodes and such semiconductor devices. The present invention relates also to a method of manufacturing the semiconductor device with such a vertical semiconductor structure.

[0002] The semiconductor devices may be roughly classified into a lateral semiconductor device that arranges its electrodes on a major surface and a vertical semiconductor device that distributes its electrodes on both major surfaces facing opposite to each other. When the vertical semiconductor device is ON, a drift current flows in the expansion direction of the depletion layers caused by the reverse bias voltage when the vertical semiconductor device is OFF. Fig. 19 is a cross section of a conventional planar n-channel vertical MOSFET. Referring now to Fig. 19, this vertical MOSFET includes a drain electrode 18; an n^+-type drain layer 11 with low resistance, to that drain electrode 18 is in electrical contact; a highly resistive n^--type drift layer 12 on n^+-type drain layer 11; a p-type base region 13a selectively formed in the surface portion of n^--type drift layer 12; a heavily doped n^+-type source region 14 selectively formed in p-type base region 13a; a gate electrode layer 16 above the extended portion of p-type base region 13a extended between n^+-type source region 14 and n^--type drift layer 12; a gate oxide film 15 between gate electrode layer 16 and the extended portion of p-type base region 13a; a source electrode 17 in common contact with the surfaces of n^+-type source region 14 and p-type base region 13a; and a drain electrode 18 on the back surface of n^+-type drain layer 11.

[0003] In the vertical semiconductor device as shown in Fig. 19, highly resistive n^--type drift layer 12 works as a region for making a drift current flow vertically when the MOSFET is in the ON-state. Highly resistive n^--type drift layer 12 is depleted when the MOSFET is in the OFF-state, resulting in a high breakdown voltage of the MOSFET. Shortening the current path in highly resistive n^--type drift layer 12 is effective for substantially reducing the on-resistance (resistance between the drain and the source) of the MOSFET, since the drift resistance is lowered. However, the short current path in n^--type drift layer 12 causes breakdown at a low voltage, since the expansion width of the depletion layer that expands from the pn-junction between p-type base region 13a and n^--type drift layer 12 is narrowed and the electric field strength soon reaches the maximum (critical) value for silicon. In the semiconductor device with a high breakdown voltage, its thick n^--type drift layer 12 inevitably causes high on-resistance and loss increase. In short, there exists a tradeoff relation between the on-resistance and the breakdown voltage of the MOSFET. This tradeoff relation between the on-resistance and the breakdown voltage exists also in the other semiconductor devices such as the IGBTs, the bipolar transistors and the diodes. The tradeoff between the on-resistance and the breakdown voltage is also hazardous for the lateral semiconductor devices, in which the flow direction of the drift current in the ON-state of the devices is different from the expansion direction of the depletion layer in the OFF-state of the device.

[0004] EP0053854, USP5216275, USP5438215 and Japanese Unexamined Laid Open Patent Application H09 (1997)-266311 disclose the semiconductor devices that include a drift layer including heavily doped n-type regions and p-type regions alternately laminated with each other to solve the foregoing problems. The alternately laminated n-type regions and p-type regions are depleted to bear the breakdown voltage in the OFF-state of the device.

[0005] Fig. 20 is a cross section of a part of the vertical MOSFET according to an embodiment of USP5216275. The vertical MOSFET of Fig. 20 is different from the vertical MOSFET of Fig. 19 in that the vertical MOSFET of Fig. 20 includes a drift layer 22, that is not a single-layered one but consisting of n-type drift regions 22a and p-type drift regions 22b alternately laminated with each other. In the figure, the reference numeral 23a designates a p-type base region, 24 an n^+-type source region, 26 a gate electrode, 27 a source electrode, and 28 a drain electrode.

[0006] Drift layer 22 is formed in the following way. At first, a highly resistive n-type layer is grown epitaxially on an n^+-type drain layer 21. The n-type drift regions 22a are formed by etching the highly resistive n-type layer to form trenches down to n^+-type drain layer 21. Then, p-type drift regions 22b are formed by epitaxially growing p-type layers in the trenches.

[0007] Hereinafter, the semiconductor device, including an alternating conductivity type drift layer that makes a current flow in the ON-state of the device and is depleted in the OFF-state of the device, will be referred to as a "semiconductor device with alternating conductivity type layer".

[0008] The dimensions described in USP5216275 are as follows. When the breakdown voltage is put in V_B, the thickness of the drift layer 22 is $0.024V_B^{1.2}$(μm). When n-type drift region 22a and p-type drift region 22b have the same thickness b and the same impurity concentration, the impurity concentration is $7.2\times10^{16}V_B^{-0.2}$/b($cm^{-3}$). If V_B is 800 V and b 5 μm, the drift layer 22 will be 73 μm in thickness and the impurity concentration 1.9×10^{16} cm^{-3}. Since the impurity concentration for the single-layered drift layer is around 2×10^{14} cm^{-3}, the on-resistance is reduced obviously. However, it is difficult for the conventional epitaxial growth techniques to bury a good quality semiconductor layer in such a narrow and deep trench (with a large aspect ratio).

[0009] The tradeoff between the on-resistance and the breakdown voltage is also hazardous commonly for

the lateral semiconductive devices. The foregoing EP0053854, USP5438215 and Japanese Unexamined Laid Open Patent Application H09(1997)-266311 disclose also the lateral semiconductor devices with an alternating conductivity type layer and the methods, common to the lateral semiconductor devices and vertical semiconductor devices, for forming the alternating conductivity type layer which employ the selective etching technique for digging trenches and the epitaxial growth technique for filling the trenches. It is not so difficult to employ the selective etching technique and the epitaxial growth technique in manufacturing the lateral semiconductor device with alternating conductivity type layer, since thin epitaxial layers are laminated one by one in manufacturing the lateral semiconductor device with alternating conductivity type layer.

[0010] However, it is difficult to employ the selective etching technique for digging trenches and the epitaxial growth technique for filling the trenches in manufacturing the vertical semiconductor devices with alternating conductivity type layer as explained with reference to USP5216275. Japanese Unexamined Laid Open Patent Application H09 (1997)-266311 describes the nuclear transformation by a neutron beam and such radioactive beams. However, the nuclear transformation that needs large facilities can not be used easily.

[0011] In view of the foregoing, it is an object of the invention to provide a semiconductor device with alternating conductivity type layer that greatly relaxes the tradeoff relation between the on-resistance and the breakdown voltage. It is another object of the invention to provide a semiconductor device with alternating conductivity type layer and with a high breakdown voltage that facilitates increasing the current capacity by reducing the on-resistance. It is still another object of the invention to provide a method for manufacturing such a semiconductor device with alternating conductivity type layer easily and with excellent mass-productivity.

[0012] According to an aspect of the invention, there is provided a semiconductor device including: a layer with low electrical resistance; a semiconductive substrate region on the layer with low electrical resistance; one or more electrodes on the surface of the semiconductive substrate region; and an electrode on the back surface of the layer with low electrical resistance; the semiconductive substrate region providing a current path when the semiconductor device is ON and being depleted when the semiconductor device is OFF; the semiconductive substrate region including regions of a first conductivity type and regions of a second conductivity type; the regions of the first conductivity type and the regions of the second conductivity type being extended in parallel to each other vertically and arranged alternately with each other horizontally; each of the regions of the first conductivity type including a plurality of second buried regions of the first conductivity type aligned vertically at a predetermined pitch; each of the regions of the second conductivity type including a plurality of first buried regions of the second conductivity type aligned vertically at the predetermined pitch.

[0013] Advantageously, the first buried regions and the second buried regions are located at almost the same depths from the surface of the semiconductive substrate region.

[0014] Advantageously, the second buried regions are located near the midpoints between the depths, at which the first buried regions are located, from the surface of the semiconductive substrate region.

[0015] Since the above described semiconductive substrate region is depleted in the OFF-state of the semiconductor device, the impurity concentrations in the first buried regions or the second buried regions can be increased. Thus, the on-resistance is lowered.

[0016] Advantageously, the spacing l_1 between the centres of the adjacent first buried regions aligned vertically is from 2 to 10 μm.

[0017] When the spacing l_1 exceeds 10 μm, heat treatment should be conducted for an extended period of time to make the first buried regions or the depletion layers which expand from the first buried regions continue to each other. When the spacing l_1 is less than 2 μm, growth of the highly resistive layer and impurity doping by ion implantation should be repeated may times, resulting in increased manufacturing steps which are hazardous for mass-production.

[0018] Advantageously, a relational expression $0.5d \leqq l_1 \leqq 2d$ holds for the spacing l_1 between the centres of the adjacent first buried regions aligned vertically and the average spacing 2d between the centres of the horizontally adjacent first buried regions.

[0019] If one assumes that the impurities diffuse evenly in all the directions, the upper buried regions and the lower buried regions continue to each other and, at the same time, the first buried regions and the second buried regions continue to each other, when $l_1=d$. If l_1 is so much different from d, heat treatment should be conducted for an extended period of time to make the upper buried regions and the lower buried regions continue to each other after the first buried regions and the second buried regions have continued to each other or to make the first buried regions and the second buried regions continue after the upper buried regions and the lower buried regions have continued to each other. Thus, l_1 so much different from d is not desirable from the view point of effective use of time. Therefore, the desirable range for l_1 is between 0.5d and 2d.

[0020] Advantageously, a relational expression l_0 l_1 holds for the spacing l_0 between the upper surface of the layer with low electrical resistance and the centre of the lowermost first buried region and the spacing l_1 between the centres of the adjacent first buried regions aligned vertically.

[0021] If l_0 is close to l_1, the highly resistive region remains with about half the original thickness left. The remaining highly resistive region causes increased on-resistance. Therefore, it is preferable for l_0 to be much

smaller than l_1.

[0022] Advantageously, the first buried regions aligned vertically continue to each other.

[0023] Since the first buried regions of the second conductivity type are disposed to expand depletion layers into the second buried regions of the first conductivity type, the vertically aligned first buried regions may be separated as far as the spaces between them are narrow enough to make the depletion layers continue. However, the first buried regions surely work as intended, when they continue to each other.

[0024] Advantageously, the second buried regions aligned vertically continue to each other.

[0025] Since the vertically aligned second buried regions provide a drift current path, the highly resistive layer between them causes increased on-resistance. Therefore, it is desirable for the vertically aligned second buried regions to continue to each other. Since the second buried regions of the first conductivity type are disposed to expand depletion layers into the first buried regions of the second conductivity type, the vertically aligned second buried regions may be separated as far as the spaces between them are narrow enough to make the depletion layers continue. However, the second buried regions surely work as intended, when they continue to each other.

[0026] Advantageously, the first buried regions and the second buried regions are shaped with stripes extending horizontally. Advantageously, the first buried regions are shaped with a lattice or a honeycomb extending horizontally, and the second buried regions are in the horizontally lattice-shaped first buried regions or in the bores of the horizontally honeycomb-shaped first buried regions. Alternatively, the second buried regions are shaped with a lattice or a honeycomb extending horizontally, and the first buried regions are in the horizontally lattice-shaped second buried regions or in the bores of the horizontally honeycomb-shaped second buried region. Advantageously, the first buried regions are distributed on the lattice points of a rectangular lattice, a triangular lattice or a hexagonal lattice, and the second buried region is between the horizontally adjacent first buried regions. Alternatively, the first buried regions are distributed on the lattice points of a rectangular lattice, a triangular lattice or a hexagonal lattice, and the second buried region is in the centre of the unit lattice of the rectangular lattice, the triangular lattice or the hexagonal lattice.

[0027] Any patterns and configurations are acceptable as far as they facilitate expanding the depletion layers into the first buried regions and the second buried regions.

[0028] Advantageously, the average spacing 2d between the centres of the horizontally adjacent first buried regions is from 2 to 20 μm.

[0029] When impurity is diffused for about 0.3 μm form the window, opened in the surface of the epitaxial layer, of 0.4 μm in width, that is the limit of the conventional lithographic technique, 2d is about 2 μm. When 2d exceeds 20 μm, the impurity concentrations should be around $2\times10^{15}cm^{-3}$ to deplete the first buried regions and the second buried regions by applying a voltage of around 300V. The impurity concentration of about $2\times10^{15}cm^{-3}$ is not so effective to reduce the on-resistance.

[0030] According to another aspect of the invention, the first buried regions and the second buried regions are formed by diffusing respective impurities into a highly resistive layer laminate epitaxially grown on the layer with low electrical resistance.

[0031] By the above described manufacturing method, the semiconductor device with alternating conductivity type layer is manufactured easily without employing such difficult steps of digging the trenches with a high aspect ratio and filling the trenches with buried regions. In the semiconductor device manufactured by the method according to the invention, impurity concentration distributions are caused in the first buried regions and the second buried regions by the impurity diffusion from limited impurity sources.

[0032] Now the present invention will be described hereinafter with reference to the accompanied drawing figures which illustrate the preferred embodiments of the invention.

Fig. 1 is a cross section of a semiconductor device with alternating conductivity type layer according to a first embodiment of the invention;

Fig. 2(a) is a cross section along A-A of the semiconductor device with alternating conductivity type layer of Fig. 1;

Fig. 2(b) is a cross section along B-B of the semiconductor device with alternating conductivity type layer of Fig.1;

Fig. 3(a) is an impurity distribution profile along A-A of Fig. 1;

Fig. 3(b) is an impurity distribution profile along C-C of Fig. 1;

Fig. 3(c) is an impurity distribution profile along D-D of Fig. 1;

Figs. 4(a) through 4(d) are cross sections describing the steps for manufacturing the MOSFET with alternating conductivity type layer according to the first embodiment of the invention;

Figs. 5(a) and 5(b) are further cross sections describing the further steps for manufacturing the MOSFET with alternating conductivity type layer according to the first embodiment of the invention;

Fig. 6 is a cross section of a modification of the MOSFET with alternating conductivity type layer according to the first embodiment of the invention;

Fig. 7 is a top plan view showing an example of planar arrangement of the first buried region and the second buried region;

Fig. 8 is a top plan view showing another example of planar arrangement of the first buried region and the second buried region;

Fig. 9 is a top plan view showing still another example of planar arrangement of the first buried region and the second buried region;

Fig. 10 is a top plan view showing a further example of planar arrangement of the first buried region and the second buried region;

Fig. 11 is a top plan view showing a still further example of planar arrangement of the first buried region and the second buried region;

Fig. 12 is a top plan view showing the other example of planar arrangement of the first buried region and the second buried region;

Fig. 13 is a cross section of a semiconductor device with alternating conductivity type layer according to a second embodiment of the invention;

Fig. 14 is a cross section of a semiconductor device with alternating conductivity type layer according to a third embodiment of the invention;

Fig. 15 is a cross section of a semiconductor device with alternating conductivity type layer according to a fourth embodiment of the invention;

Fig. 16 is a cross section of a semiconductor device with alternating conductivity type layer according to a fifth embodiment of the invention;

Fig. 17 is a cross section of a semiconductor device with alternating conductivity type layer according to a sixth embodiment of the invention;

Fig. 18 is a cross section of a semiconductor device with alternating conductivity type layer according to a seventh embodiment of the invention;

Fig. 19 is a cross section of a conventional planar n-channel vertical MOSFET; and,

Fig. 20 is a cross section of a part of the vertical MOSFET according to an embodiment of USP5216275.

First embodiment

[0033] Fig. 1 is a cross section of a semiconductor device with alternating conductivity type layer according to a first embodiment of the invention. Fig. 2(a) is a cross section along A-A of the semiconductor device with alternating conductivity type layer of Fig. 1. Fig. 2(b) is a cross section along B-B of the semiconductor device with alternating conductivity type layer of Fig. 1.

[0034] Referring now to Fig. 1, a semiconductive substrate region 32 is on an n^+-type drain layer 31 with low resistance. Semiconductive substrate region 32 includes a highly resistive n^--type layer 32a, a plurality of vertical alignments of n-type buried regions 32b and a plurality of vertical alignments of p-type buried regions 32c. The vertical alignments of n-type buried regions 32b and the vertical alignments of p-type buried regions 32c are alternately arranged with each other horizontally. An n-type channel layer 32d is in contact with the uppermost n-type buried region 32b. A p-type base region 33a is in contact with the uppermost p-type buried region 32c. An n^+-type source region 34 and a heavily doped p^+-type well region 33b are in p-type base region 33a. A gate electrode layer 36 is above the extended portion of p-type base region 33a extended between n^+-type source region 34 and n-type channel layer 32d with a gate insulation film 35 interposed in-between. A source electrode 37 is in contact commonly with n^+-type source region 34 and p^+-type well region 33b. A drain electrode 38 is on the back surface of n^+-type drain layer 31. Very often, source electrode 37 is extended over gate electrode layer 36 with an insulation film 39 interposed in-between as shown in Fig. 1. Although the drift current flows through n-type buried regions 32b and highly resistive n^--type layers 32a, the semiconductive substrate region including p-type buried regions 32c will be collectively referred to hereinafter as the drift layer.

[0035] Broken lines in Fig. 1 indicate the planes, at that the formation of the semiconductive substrate region 32 is interrupted and from that impurities are implanted. The n-type buried regions 32b and p-type buried regions 32c are formed by impurity diffusion from the respective impurity sources implanted into the central portions of n-type buried regions 32b and p-type buried regions 32c. Although the pn-junctions between n-type buried regions 32b and p-type buried regions 32c are represented by curves in Fig. 1 (curved surfaces three-dimensionally) due to their formation technique described above, the pn-junctions between n-type buried regions 32b and p-type buried regions 32c are straitened (to be flat planes three-dimensionally) gradually as the heat treatment period for diffusion is extended.

[0036] As described in Fig. 2(a), n-type buried regions 32b and p-type buried regions 32c extend horizontally as stripes. In Fig. 2(a), n-type buried regions 32b and p-type buried regions 32c are in contact to each other. In Fig. 2 (b), i.e. along B-B of Fig. 1, n-type buried regions 32b and p-type buried regions 32c are not in contact to

each other with highly resistive n-type layer 32a left in-between. Highly resistive n-type layer 32a left between n-type buried regions 32b and p-type buried regions 32c may be narrowed and fades away ultimately by extending the time period for the heat treatment subsequent to ion implantation.

[0037] Fig. 3(a) is an impurity distribution profile along A-A of Fig. 1. Fig. 3(b) is an impurity distribution profile along C-C of Fig. 1. Fig. 3(c) is an impurity distribution profile along D-D of Fig. 1. In these figures, the vertical axis represents the logarithmic impurity concentration. In Fig. 3(a), the impurity distributions caused by the diffusion from the respective impurity sources of n-type buried regions 32b and p-type buried regions 32c arranged alternately are repeated. In Fig. 3(b), the impurity distributions caused by the diffusion from the diffusion sources of n-type buried regions 32b are continuous and repeated vertically above n^+-type drain layer 31 with low resistance. Impurity distribution is also caused in n-type channel region 32d on the uppermost n-type buried region 32b by the diffusion from the surface of n-type channel region. In Fig. 3(c), the impurity distributions caused by the diffusion from the diffusion sources of p-type buried regions 32c are continuous and repeated vertically above n^+-type drain layer 31 with low resistance. Impurity distributions are also caused in p-type base region 33a and p^+-type well region 33b continuous to the uppermost p-type buried region 32c by the diffusion from their surfaces.

[0038] The semiconductor device with alternating conductivity type layer of Fig. 1 works as follows. When a predetermined positive voltage is applied to gate electrode layer 36, an inversion layer is caused in the surface portion of p-type base region 33a beneath gate electrode layer 36. The electrons injected to n-type channel region 33b from n^+-type source region 34 via the inversion layer reach n^+-type drain layer 31 via n-type buried regions 32b, resulting in electrical conduction between drain electrode 38 and source electrode 37.

[0039] As the positive voltage is removed from gate electrode layer 36, the inversion layer induced in the surface portion of p-type base region 33a vanishes, and the drain and the source are electrically disconnected from each other. As the reverse bias voltage is further boosted, depletion layers expand into n-type buried regions 32b and p-type buried regions 32c from the pn-junctions Ja between p-type base regions 33a and n-type channel regions 32d, the pn-junctions Jb between p-type buried regions 32c and n-type buried regions 32b and the pn-junctions Jc between p-type buried regions 32c and highly resistive n-type layer 32a. Thus, n-type buried regions 32b and p-type buried regions 32c are depleted.

[0040] The n-type buried regions 32b are depleted very quickly, since the edges of the depletion layers from the pn-junctions Jb and Jc advance in the width direction of n-type buried regions 32b and since depletion layers also expand into n-type buried regions 32b from p-type buried regions 32c on both sides of n-type buried regions 32b. Therefore, n-type buried regions 32b may be heavily doped.

[0041] The p-type buried regions 32c are depleted simultaneously with n-type buried regions 32b. The p-type buried regions 32c are depleted very quickly, since depletion layers expand into p-type buried regions 32c from their both sides. Since the edges of the depletion layer from p-type buried region 32c enter adjacent n-type buried regions 32b by virtue of the alternating arrangement of p-type buried regions 32c and n-type buried regions 32b, the total width occupied by p-type buried regions 32c for forming depletion layers may be halved. Accordingly, the cross sectional area of n-type buried regions 32b may be widened.

[0042] The dimensions and the impurity concentrations for the MOSFET of the 300 V class are as follows. The specific resistance of n^+-type drain layer 31 is 0.01 Ω-cm. The thickness of n^+-type drain layer 31 is 350 μm. The specific resistance of highly resistive n^--type drain layer 32a is 10 Ω-cm. The thickness of drift layer 32 is 25 μm (5 μm each for I_0, I_1, I_2, ···). The n-type buried region 32b and p-type buried region 32c are 5 μm in width: the spacing between the centres of the buried regions with the same conductivity type is 10 μm. The average impurity concentration in the n-type buried regions 32b and p-type buried regions 32c is $7\times10^{15}cm^{-3}$. The diffusion depth of p-type base region 33a is 1 μm. The surface impurity concentration of p-type base region 33a is 3×10^{18} cm^{-3}. The diffusion depth of n^+-type source region 34 is 0.3 μm. The surface impurity concentration of n^+-type source region 34 is 1×10^{20} cm^{-3}.

[0043] For providing the conventional vertical MOSFET with the breakdown voltage of the 300 V class, it is necessary for its single-layered highly resistive drift layer to contain the impurity of around $2\times10^{14}cm^{-3}$ in concentration and to be 40 μm in thickness. In the MOSFET with alternating conductivity type layer according to the first embodiment of the invention, its on-resistance is reduced to the one fifth of that of the conventional vertical MOSFET by increasing the impurity concentration in n-type buried regions 32b and by thinning drift layer 32 corresponding to the increment of the impurity concentration.

[0044] The on-resistance is further reduced and the tradeoff relation between the on-resistance and the breakdown voltage is improved by further thinning the width of n-type buried regions 32b and by further increasing its impurity concentration.

[0045] The MOSFET with alternating conductivity type layer according to the first embodiment of the invention and the conventional MOSFET with alternating conductivity type layer of Fig. 20 are different from each other especially in the method of forming drift layer 32 and the resulting structure of drift layer 32. To describe in other words, since n-type buried regions 32b and p-type buried regions 32c of drift layer 32 in the MOSFET according to the invention are formed by impurity diffu-

sion, impurity distributions are caused in drift layer 32 by the diffusion.

[0046] Figs. 4(a) through 4(d) and Figs. 5(a) and 5(b) are cross sections describing the steps for manufacturing the MOSFET with alternating conductivity type layer according to the first embodiment of the invention.

[0047] Referring now to Fig. 4(a), a highly resistive n^--type layer 32a is grown on an n^+-type drain layer 32 that works as an n-type substrate with low resistance. In this embodiment, the thickness l_0 of n-type layer 32a deposited at first is set at 4 μm.

[0048] Referring now to Fig. 4(b), a photoresist mask pattern 1 is formed on the n^--type layer 32a and boron ions (hereinafter referred to as "B ions" 2 are implanted under the acceleration voltage of 50 keV and at the dose amount of $1\times10^{13}cm^{-2}$. The implanted B ions are designated by the reference numeral 3.

[0049] Referring now to Fig. 4(c), a photoresist mask pattern 2 is formed on the n^--type layer 32a and phosphorus ions (hereinafter referred to as "P ions" 5 are implanted under the acceleration voltage of 50 keV and at the dose amount of $1\times10^{13}cm^{-2}$. The implanted P ions are designated by the reference numeral 6.

[0050] Referring now to Fig. 4(d), an additional highly resistive n^--type layer 32a is grown to the thickness of l_1, photoresist mask patterns are formed, and B and P ions are implanted in the similar manners as described above with reference to Figs. 4(a) through 4(c). These steps are repeated until drift layer 32 has been grown to the predetermined thickness. In this embodiment, the thickness l_1 of the additional highly resistive n^--type layers is set at 5 μm and three additional n^--type layers are laminated. And, a layer for forming a surface portion is grown on the uppermost highly resistive n^--type layer.

[0051] Referring now to Fig. 5(a), n-type buried regions 32b and p-type buried regions 32c are formed by diffusing the implanted impurities by the heat treatment conducted at 1150 °C for 5 hr. The impurities diffuse for about 3 μm by this heat treatment, resulting in contact of n-type buried regions 32b and p-type buried regions 32c to each other. The final shapes of n-type buried regions 32b and p-type buried regions 32c may be varied by changing the shape of the masks for ion implantation, the dose amounts of the impurities and the time period of the heat treatment.

[0052] Referring now to Fig. 5(b), n-type channel region 32d, p-type base region 33a, n^+-type source region 34 and p^+-type well region 33b are formed in the surface portion in the same manner as those in the conventional vertical MOSFET by selective impurity ion implantation and by the subsequent heat treatment.

[0053] Then, gate insulation film 35 is formed by thermal oxidation. Gate electrode layer 36 is formed by depositing polycrystalline silicon film by the vacuum CVD technique and by the subsequent photolithographic process. Then, insulation film 39 is deposited and windows are opened through insulation film 39. Source electrode 37, drain electrode 38 and the not shown metallic portion of the gate electrode are formed by depositing an aluminum alloy layer and by patterning the deposited aluminum alloy layer. Thus, the vertical MOSFET as shown in Fig. 1 is completed.

[0054] Technically, it is quite general to form buried regions by growing epitaxial layers of several m in thickness and by thermally diffusing implanted impurity ions. The technique employed in the invention facilitates manufacturing the MOSFET with alternating conductivity type layer that improves the tradeoff relation between the on-resistance and the breakdown voltage without using such a difficult technique for forming trenches with a large aspect ratio and for filling each trench with a high-quality epitaxial layer.

[0055] If highly resistive n-type layer 32a remaining below n-type buried region is thick, the on-resistance will be high. Therefore, the thickness l_0 of the epitaxial layer on n^+-type drain layer 31 is set to be thinner than the thickness l_1 of the next epitaxial layer.

[0056] Fig. 6 is a cross section of a modification of the MOSFET with alternating conductivity type layer according to the first embodiment of the invention. This modified MOSFET is manufactured by extending the time period for the heat treatment conducted subsequently to the impurity ion implantation and the epitaxial growth described with reference to Fig. 4(d). Due to the extended heat treatment, highly resistive n^--type layer 32a has vanished and adjacent n-type buried regions 32b and p-type buried regions 32c are contacting with each other almost over their entire side faces, resulting in flat boundaries. The resulting flat boundaries between n-type buried regions 32b and p-type buried regions 32c are expressed by straight lines in Fig. 6.

[0057] The cross section shown in Fig.6 for the modification resembles the cross section shown in Fig. 20 for the conventional MOSFET. However, their internal semiconductor structure are different from each other. In Fig. 20, the impurity concentration is almost uniform in each epitaxial layer, since the epitaxial layers are formed by growing a first epitaxial layer and by filling the trenches dug in the first epitaxial layer with second epitaxial layers. In contrast, the impurity distribution profiles along E-E, F-F and G-G of Fig.6 are essentially the same with those described in Fig. 3(a), Fig. 3(b), and Fig. 3(c), respectively. The impurity distribution due to highly resistive n^--type layer 32a does not appear in the profiles along E-E, F-F and G-G of Fig.6, since any resistive n^--type layer 32a is not remaining in Fig.6. The impurity distribution profile along E-E of Fig.6 includes the impurity distributions across n-type buried regions 32b and p-type buried regions 32c alternately arranged with each other horizontally. The impurity distribution profile along F-F of Fig.6 includes the impurity distribution across n^+ drain layer 31, cyclic concentration change due to the diffusion from the sources in n-type buried regions 32b and the impurity distribution across n-type channel region 32d in the surface portion. The impurity distribution profile along G-G of Fig.6 includes

the impurity distribution across n^+ drain layer 31, cyclic concentration change due to the diffusion from the sources in p-type buried regions 32c, the impurity distribution across p-type base region 32a and the impurity distribution across p^+-type well region 33b in the surface portion.

[0058] Although n-type buried regions 32b and p-type buried regions 32c are arranged in stripes horizontally in the first embodiment of the invention, n-type buried regions 32b and p-type buried regions 32c may be arranged in different fashions. Figs. 7 through 12 show various planar arrangements of n-type buried regions 32b and p-type buried regions 32c. In Fig. 7, a matrix of rectangular n-type buried regions 32b is arranged in p-type buried region 32c. In Fig. 8, a matrix of rectangular p-type buried regions 32c is arranged in n-type buried region 32b. Alternatively, n-type buried region 32b or p-type buried region 32c is shaped with a honeycomb, the bores of that are filled with p-type buried regions 32c or n-type buried regions 32b.

[0059] Figs. 9 through 12 show the examples of scattered arrangement. In Fig. 9, p-type buried regions 32c are arranged at the lattice points of a square lattice and n-type buried region 32b is arranged between adjacent p-type buried regions 32c. In Fig. 10, p-type buried regions 32c are arranged at the lattice points of a square lattice and n-type buried region 32b is arranged in the centre of each unit lattice. In Fig. 11, p-type buried regions 32c are arranged at the lattice points of a triangular lattice and n-type buried region 32b is arranged between adjacent p-type buried regions 32c. In Fig. 12, p-type buried regions 32c are arranged at the lattice points of a triangular lattice and n-type buried region 32b is arranged in the centre of the unit lattice. In these arrangements, the spacing between n-type buried region 32b and p-type buried region 32c is narrowed by extending the time period for the heat treatment conducted subsequently to the epitaxial growth and the impurity ion implantation. In some cases, a p-type layer may be used in substitution for highly resistive n^--type layer 32a. Other various repetitive arrangements may be adopted.

[0060] It is not always necessary to shape p-type base region 33a in the surface portion and p-type buried region 32c with similar planar patterns. The p-type base region 33a and p-type buried region 32c may be shaped with quite different respective patterns as far as they are connected to each other For example, when p-type base region 33a and p-type buried region 32c may be shaped with respective stripe patterns, which extend perpendicularly to each other.

[0061] In any arrangement, the contact area between n-type buried regions 32b and p-type buried regions 32c is widened gradually as the time period for thermal diffusion is extended and highly resistive n^--type layer 32a is narrowed gradually until it finally vanishes.

[0062] In the first embodiment, heat treatment is conducted for connecting the upper and lower n-type buried regions 32b. When the highly resistive layer is n^--type layer 32a, it is not always necessary to connect the upper and lower n-type buried regions 32b. However, n^--type layer 32a remaining between n-type buried regions 32b increases the on-resistance. It is not always necessary to connect the upper and lower p-type buried regions 32c as far as they are spaced apart for the distance short enough for the depletion layers to join each other.

Second embodiment

[0063] Fig. 13 is a cross section of a semiconductor device with alternating conductivity type layer according to a second embodiment of the invention.

[0064] Referring now to Fig. 13, a drift layer 42 is on an n^+-type drain layer 41 with low resistance. Drift layer 42 includes a highly resistive layer 42a, a plurality of vertical alignments of n-type buried regions 42b and a plurality of vertical alignments of p-type buried regions 42c. The vertical alignments of n-type buried regions 42b and the vertical alignments of p-type buried regions 42c are alternately arranged with each other horizontally. In the surface portion of drift layer 42, n-type channel layers 42d are formed on the uppermost n-type buried regions 42b and p-type base regions 43a on the uppermost p-type buried regions 42c. An n^+-type source region 44 and a heavily doped p^+-type well region 43b are in p-type base region 43a. A gate electrode layer 46 is above the extended portion of p-type base region 43a extended between n^+-type source region 44 and n-type channel layer 42d with a gate insulation film 45 interposed in-between. A source electrode 47 is in common contact with n^+-type source region 44 and heavily doped p^+-type well region 43b. A drain electrode 48 is on the back surface of n^+-type drain layer 41.

[0065] The MOSFET with alternating conductivity type layer according to the second embodiment of the invention is different from the MOSFET with alternating conductivity type layer according to the first embodiment in the way of forming its drift layer and the resulting structure of the drift layer. To describe in other words, n-type buried regions 42b and p-type buried regions 42c are formed by the diffusion of the respective impurities implanted in the surface portions of different epitaxial layers.

[0066] It is not always necessary to implant the impurities for the n-type buried regions and the p-type buried regions at the same depth similarly as in the first embodiment. The n-type buried regions 42b and p-type buried regions 42c may be at different depths.

[0067] The MOSFET with alternating conductivity type layer according to the second embodiment of the invention exhibits the same effects as those of the MOSFET with alternating conductivity type layer according to the first embodiment. The MOSFET with alternating conductivity type layer that improves the tradeoff relation between the on-resistance and the breakdown voltage according to the second embodiment is manufac-

tured by the quite general epitaxial growth and impurity diffusion techniques without using such a difficult technique for forming trenches with a large aspect ratio and for filling each trench with a high-quality epitaxial layer.

[0068] The n-type buried regions and the p-type buried regions may be arranged two dimensionally in a stripe pattern, in a lattice pattern, or in a scattered fashion in the second and following embodiments in the same manner as in the first embodiment.

[0069] In the second embodiment, it is not always necessary for the highly resistive layer to be of n-type and a highly resistive p-type layer is acceptable, since n-type buried regions 42b are in contact with n^+-type drain layer 41. When the highly resistive lay is of p-type, it is not necessary for the upper and lower p-type buried regions 42c to be in contact with each other.

Third embodiment

[0070] Fig. 14 is a cross section of a semiconductor device with alternating conductivity type layer according to a third embodiment of the invention.

[0071] The semiconductor device shown in Fig. 14 is a UMOSFET that includes trench gates. The gate structure of the UMOSFET is different from that of the MOSFET according to the first embodiment. Referring now to Fig. 14, trenches are dug in the surface portion of a drift layer 52. A gate electrode layer 56 is surrounded by a gate insulation film 55 in the trench. In the remaining surface portion of drift layer 52, p-type base layers 53a are formed in the depth as shallow as that of gate electrode layer 56, and n^+ source regions 54 are formed along the upper edges of gate electrode layers 56. A thick insulation film 59 covers gate electrode layers 56. Drift layer 52 includes a plurality of vertical alignments of n-type buried regions 52b and a plurality of vertical alignments of p-type buried regions 52c similarly as in the foregoing embodiments. The vertical alignments of n-type buried regions 52b and the vertical alignments of p-type buried regions 52c are alternately arranged with each other horizontally.

[0072] In the third embodiment, n-type buried region 52b and p-type buried region 52c have the dimensions and impurity concentrations almost same with those in the first embodiment. When a reverse bias voltage is applied, drift layer 52 is depleted to bear the breakdown voltage.

[0073] Since n-type buried regions 52b and p-type buried regions 52c are easily depleted, they can be doped heavily. Since drift layer 52 can be thinned by virtue of the heavy doping to n-type buried regions 52b and p-type buried regions 52c, the on-resistance is lowered greatly and the tradeoff relation between the on-resistance and the breakdown voltage is improved. By using the quite general techniques such as epitaxial growth and impurity diffusion, the UMOSFET with alternating conductivity type layer that improves the tradeoff relation between the on-resistance and the breakdown voltage is manufactured easily.

Fourth embodiment

[0074] Fig. 15 is a cross section of a semiconductor device with alternating conductivity type layer according to a fourth embodiment of the invention.

[0075] The semiconductor device shown in Fig. 14 is an n-channel IGBT. The drain layer structure of the IGBT is different from that of the MOSFET according to the first embodiment. In detail, this n-channel IGBT is obtained by adopting a binary-layer structure consisting of a p^+-type drain layer 61a and an n^+-type buffer layer 61b in substitution for single-layered n^+-type drain layer 21 of the MOSFET with alternating conductivity type layer. In some cases, n^+-type buffer layer 61b may be omitted. The IGBT of Fig. 4 includes a drift layer 62 including a plurality of vertical alignments of n-type buried regions 62b and a plurality of vertical alignments of p-type buried regions 62c similarly as in the foregoing embodiments. The vertical alignments of n-type buried regions 62b and the vertical alignments of p-type buried regions 62c are alternately arranged with each other horizontally.

[0076] Since the IGBT is a semiconductor device of conductivity modulation type based on minority carrier injection, its on-resistance is much smaller than that of the MOSFET based on the drift of majority carriers. The on-resistance of the IGBT is further reduced greatly by thinning drift layer 62.

[0077] A p-type substrate with low resistance is used for p^+-type drain layer 61a. An epitaxial layer for n^+-type buffer layer 61b is grown on the p-type substrate with low resistance and, then, drift layer 62 is formed on n^+-type buffer layer 61b by epitaxial growth and impurity diffusion.

[0078] The techniques employed in the fourth embodiment facilitate manufacturing the IGBT with alternating conductivity type layer that improves the tradeoff relation between the on-resistance and the breakdown voltage without using such a difficult technique for forming trenches with a large aspect ratio and for filling each trench with a high-quality epitaxial layer.

Fifth embodiment

[0079] Fig. 16 is a cross section of a semiconductor device with alternating conductivity type layer according to a fifth embodiment of the invention.

[0080] The semiconductor device of Fig. 16 is a diode that includes an n^+-type cathode layer 71 with low resistance and a drift layer 72. Drift layer 72 includes a highly resistive n^--type layer 72a, a plurality of vertical alignments of n-type buried regions 72b and a plurality of vertical alignments of p-type buried regions 72c. The vertical alignments of n-type buried regions 72b and the vertical alignments of p-type buried regions 72c are alternately arranged with each other horizontally. A p^+-type anode layer 73 is on drift layer 72. An anode elec-

trode 78 is in contact with p^+-type anode layer 73. A cathode electrode 77 is in contact with n^+-type cathode layer 71.

[0081] In the fifth embodiment, n-type buried regions 72b and p-type buried regions 72c have the dimensions and impurity concentrations almost same with those in the first embodiment. When a reverse bias voltage is applied, drift layer 72 is depleted to bear the breakdown voltage.

[0082] Since n-type buried regions 72b and p-type buried regions 72c are easily depleted, they can be doped heavily. Since drift layer 72 can be thinned by virtue of the heavy doping to n-type buried regions 52b and p-type buried regions 52c, the on-resistance is lowered greatly and the tradeoff relation between the on-resistance and the breakdown voltage is improved.

[0083] Steps similar to those described with reference to Figs. 4(a) through 4(d) are employed for manufacturing the diode of Fig. 16. Then, p^+-type anode layer 73 is formed by ion implantation and subsequent diffusion. Finally, anode electrode 78 and cathode electrode 77 are formed.

[0084] Thus, the diode that exhibits a high breakdown voltage and a low on-resistance is manufactured easily by quite general epitaxial growth and subsequent impurity diffusion.

Sixth embodiment

[0085] Fig. 17 is a cross section of a semiconductor device with alternating conductivity type layer according to a sixth embodiment of the invention.

[0086] The semiconductor device of Fig. 17 is another diode including a drift layer 82, that is different from drift layer 72 of the fifth embodiment. Although drift layer 82 includes a highly resistive n^--type layer 82a, a plurality of vertical alignments of n-type buried regions 82b and a plurality of vertical alignments of p-type buried regions 82c, the lowermost plane and the uppermost plane, in which the impurity concentrations are highest, contact with an n^+-type cathode layer 81 and a p^+-type anode layer 83, respectively.

[0087] In the sixth embodiment, n-type buried regions 82b and p-type buried regions 82c have the dimensions and impurity concentrations almost same with those in the first embodiments. When a reverse bias voltage is applied, drift layer 82 is depleted to bear the breakdown voltage.

[0088] The diode of Fig. 17 greatly reduces its on-resistance and improves the tradeoff relation between the breakdown voltage and the on-resistance in the same way as the diode of Fig. 16 does.

[0089] The diode that exhibits a high breakdown voltage and a low on-resistance is manufactured easily in the same way as the diode of Fig. 16.

Seventh embodiment

[0090] Fig. 18 is a cross section of a semiconductor device with alternating conductivity type layer according to a seventh embodiment of the invention.

[0091] The semiconductor device of Fig. 18 is a Schottky diode that includes an n^+-type cathode layer 91 and a drift layer 92. Drift layer 92 includes a highly resistive n^--type layer 92a, a plurality of vertical alignments of n-type buried regions 92b and a plurality of vertical alignments of p-type buried regions 92c. The vertical alignments of n-type buried regions 92b and the vertical alignments of p-type buried regions 92c are alternately arranged with each other horizontally. Some parts of highly resistive n^--type layers 92a are remaining in the surface portion of drift layer 92, and the uppermost p-type buried regions 92c are extended to the surface of drift layer 92. A Schottky electrode 98 is on drift layer 92 such that Schottky barrier is formed between the Schottky electrode 98 and the remaining portion of highly resistive n^--type layer 92a remaining in the surface portion of drift layer 92. A cathode electrode 97 is on the back surface of n^+-type cathode layer 91.

[0092] In the Schottky diode with alternating conductivity type layer according to the seventh embodiment, n-type buried regions 92b and p-type buried regions 92c have the dimensions and impurity concentrations almost same with those in the first embodiments. When a reverse bias voltage is applied, drift layer 92 is depleted to bear the breakdown voltage.

[0093] Since n-type buried regions 92b and p-type buried regions 92c are easily depleted, they can be doped heavily. Since drift layer 92 can be thinned by virtue of the heavy doping to n-type buried regions 92b and p-type buried regions 92c, the on-resistance is lowered greatly and the tradeoff relation between the on-resistance and the breakdown voltage is improved.

[0094] Steps similar to those described with reference to Figs. 4(a) through 4(d) are employed for manufacturing the Schottky diode of Fig. 18. Finally, Schottky electrode 98 and cathode electrode 97 are formed.

[0095] Thus, the Schottky diode that exhibits a high breakdown voltage and a low on-resistance is manufactured easily by quite general epitaxial growth and subsequent impurity diffusion.

[0096] The semiconductor structure with alternating conductivity type layer according to the invention is applicable to almost all the semiconductor devices such as the MOSFET, IGBT, diode, bipolar transistor, JFET, thyristor, MESFET, and HEMT. The conductivity types may be exchanged appropriately.

[0097] As explained above, the semiconductor device according to the invention includes a layer with low electrical resistance; a semiconductive substrate region on the layer with low electrical resistance; one or more electrodes on the surface of the semiconductive substrate region; and an electrode on the back surface of the layer with low electrical resistance; the semiconductive sub-

strate region providing a current path when the semiconductor device is ON and being depleted when the semiconductor device is OFF; the semiconductive substrate region including regions of a first conductivity type and regions of a second conductivity type; the regions of the first conductivity type and the regions of the second conductivity type being extended in parallel to each other vertically and arranged alternately with each other horizontally; each of the regions of the first conductivity type including a plurality of second buried regions of the first conductivity type aligned vertically at a predetermined pitch; each of the regions of the second conductivity type including a plurality of first buried regions of the second conductivity type aligned vertically at the predetermined pitch.

[0098] The semiconductor device of the invention is manufactured by the method that includes the steps of epitaxially growing a highly resistive layer laminate on the layer with low resistance, and diffusing impurities into the highly resistive layer laminate to form the first buried regions and the second buried regions. The semiconductor device and its manufacturing method according to the invention exhibit the following effects.

[0099] By using the quite general techniques such as epitaxial growth and impurity diffusion, a characteristic alternating conductivity type layer has been realized easily without using such a difficult technique for forming trenches with a large aspect ratio and for filling each trench with a high-quality epitaxial layer.

[0100] The resulting easy depletion of the first buried regions and the second buried regions and the resulting increased impurity concentrations in the first buried regions and the second buried regions facilitate thinning the semiconductive substrate region that includes the alternating conductivity type layer, further resulting in greatly lowered on-resistance, e.g. lowered by 80% from the conventional value, and an improved tradeoff relation between the on-resistance and the breakdown voltage.

[0101] By applying the present invention to the power devices, novel semiconductor power devices which facilitate dramatically reducing the electrical power loss are realized.

Claims

1. A semiconductor device comprising:

   a layer with low electrical resistance;
   a semiconductive substrate region on the layer with low electrical resistance;
   one or more electrodes on the surface of the semiconductive substrate region; and
   an electrode on the back surface of the layer with low electrical resistance;
   the semiconductive substrate region providing a current path when the semiconductor device is ON and being depleted when the semiconductor device is OFF;
   the semiconductive substrate region comprising regions of a first conductivity type and regions of a second conductivity type;
   the regions of the first conductivity type and the regions of the second conductivity type being extended in parallel to each other vertically and arranged alternately with each other horizontally;
   each of the regions of the first conductivity type comprising a plurality of second buried regions of the first conductivity type aligned vertically at a predetermined pitch;
   each of the regions of the second conductivity type comprising a plurality of first buried regions of the second conductivity type aligned vertically at the predetermined pitch.

2. The semiconductor device according to Claim 1, wherein the first buried regions and the second buried regions are located at almost the same depths from the surface of the semiconductive substrate region.

3. The semiconductor device according to Claim 1, wherein the second buried regions are located near the midpoints between the depths, at which the first buried regions are located, from the surface of the semiconductive substrate region.

4. The semiconductor device according to any of Claims 1 through 3, wherein the spacing l_1 between the centres of the adjacent first buried regions aligned vertically is from 2 to 10 μm.

5. The semiconductor device according to any of Claims 1 through 4, wherein a relational expression $0.5d \leqq l_1 \leqq 2d$ holds for the spacing l_1 between the centres of the adjacent first buried regions aligned vertically and the average spacing 2d between the centres of the horizontally adjacent first buried regions.

6. The semiconductor device according to any of Claims 1 through 5, wherein a relational expression $l_0\ l_1$ holds for the spacing l_0 between the upper surface of the layer with low electrical resistance and the centre of the lowermost first buried region and the spacing l_1 between the centres of the adjacent first buried regions aligned vertically.

7. The semiconductor device according to any of Claims 1 through 6, wherein the first buried regions aligned vertically continue to each other.

8. The semiconductor device according to any of Claims 1 through 7, wherein the second buried re-

gions aligned vertically continue to each other.

9. The semiconductor device according to any of Claims 1 through 8, wherein the first buried regions and the second buried regions are shaped with stripes extending horizontally.

10. The semiconductor device according to any of Claims 1 through 8, wherein the first buried regions are shaped with a lattice or a honeycomb extending horizontally.

11. The semiconductor device according to Claim 10, wherein the second buried regions are in the horizontally lattice-shaped first buried regions or in the bores of the horizontally honeycomb-shaped first buried regions.

12. The semiconductor device according to any of Claims 1 through 8, wherein the second buried regions are shaped with a lattice or a honeycomb extending horizontally.

13. The semiconductor device according to Claim 12, wherein the first buried regions are in the horizontally lattice-shaped second buried regions or in the bores of the horizontally honeycomb-shaped second buried region.

14. The semiconductor device according to any of Claims 1 through 8, wherein the first buried regions are distributed horizontally.

15. The semiconductor device according to Claim 14, wherein the first buried regions are distributed on the lattice points of a rectangular lattice, a triangular lattice or a hexagonal lattice.

16. The semiconductor device according to Claim 15, wherein the second buried region is between the horizontally adjacent first buried regions.

17. The semiconductor device according to Claim 15, wherein the second buried region is in the centre of the unit lattice of the rectangular lattice, the triangular lattice or the hexagonal lattice.

18. The semiconductor device according to any of Claims 1 through 17, wherein the average spacing 2d between the centres of the horizontally adjacent first buried regions is from 2 to 20 μm.

19. The semiconductor device according to any of Claims 1 through 18, wherein the first buried regions and the second buried regions exhibit respective concentration distributions caused by diffusion from respective limited impurity sources.

20. The method of manufacturing the semiconductor device including a layer with low electrical resistance, a semiconductive substrate region on the layer with low electrical resistance, one or more electrodes on the surface of the semiconductive substrate region, and an electrode on the back surface of the layer with low electrical resistance, the semiconductive substrate region providing a current path when the semiconductor device is ON and being depleted when the semiconductor device is OFF, the semiconductive substrate region including regions of a first conductivity type and regions of a second conductivity type, the regions of the first conductivity type and the regions of the second conductivity type being extended in parallel to each other vertically and arranged alternately with each other horizontally, each of the regions of the first conductivity type including a plurality of second buried regions of the first conductivity type aligned vertically at a predetermined pitch, each of the regions of the second conductivity type including a plurality of first buried regions of the second conductivity type aligned vertically at the predetermined pitch, the method comprising the steps of:

(a) epitaxially growing a highly resistive layer laminate, including scattered sources of an impurity of the first conductivity type and scattered sources of an impurity of the second conductivity type, on the layer with low electrical resistance; and
(b) diffusing the impurities into the highly resistive layer laminate, whereby to form the first buried regions and the second buried regions.

21. The method according to Claim 20, wherein, the step (a) comprises the steps of:

(a-1) epitaxially growing a highly resistive layer;
(a-2) implanting sources of the impurity of the first conductivity type and sources of the impurity of the second conductivity type in the surface portion of the highly resistive layer; and
(a-3) repeating the steps (a-1) and (a-2) until the highly resistive layer laminate reaches a predetermined thickness.

22. The method according to Claim 20, wherein the step (a) comprises the steps of:

(a-1) epitaxially growing a highly resistive layer;
(a-2) implanting sources of the impurity of the first conductivity type or sources of the impurity of the second conductivity type in the surface portion of the highly resistive layer;
(a-3) epitaxially growing an additional highly resistive layer on the highly resistive layer;
(a-4) implanting sources of the impurity of the

second conductivity type or sources of the impurity of the first conductivity type in the surface portion of the additional highly resistive layer; and

(a-5) repeating the steps (a-1) through (a-4) until the highly resistive layer laminate reaches a predetermined thickness.

Fig. 1

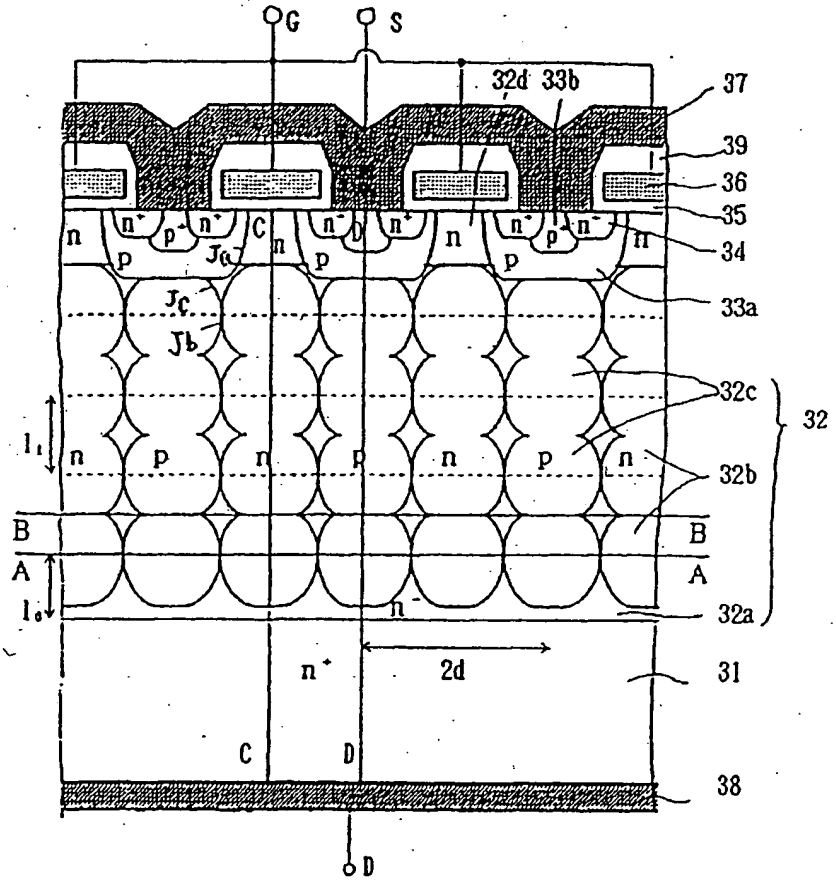


Fig. 2 (a)

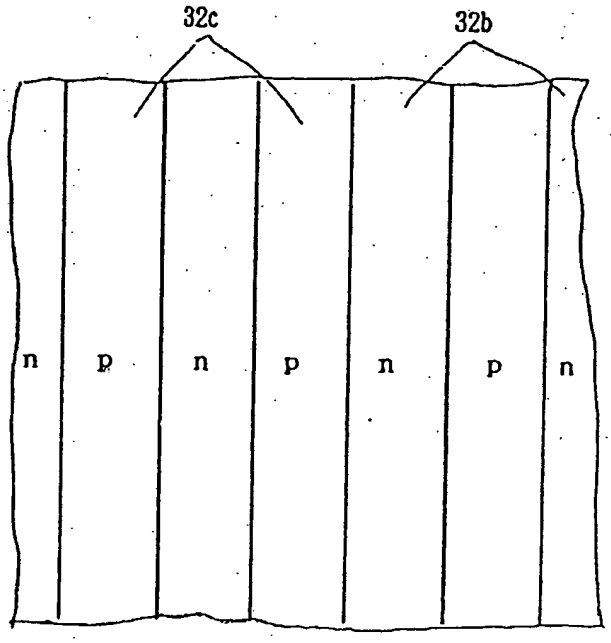


Fig. 2 (b)

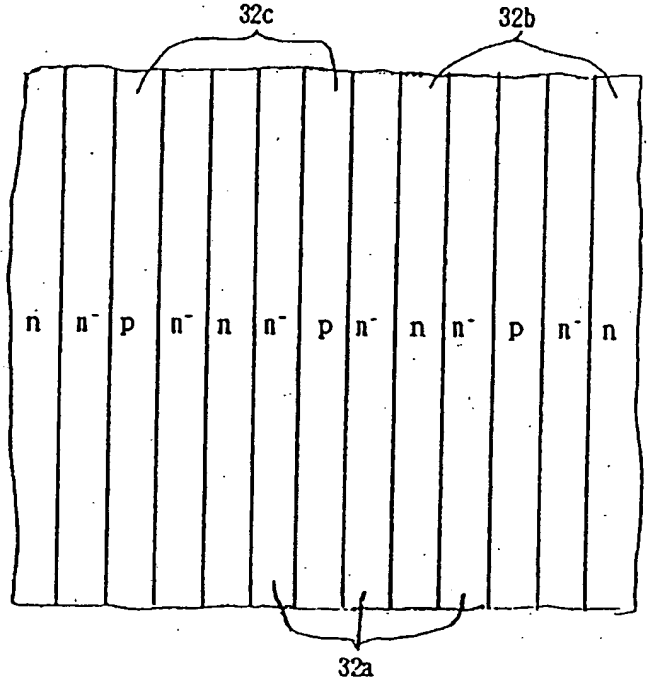


Fig.3(a)

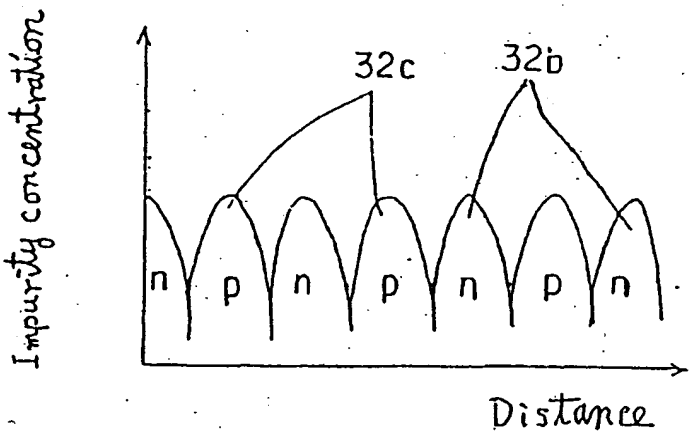


Fig.3(b)

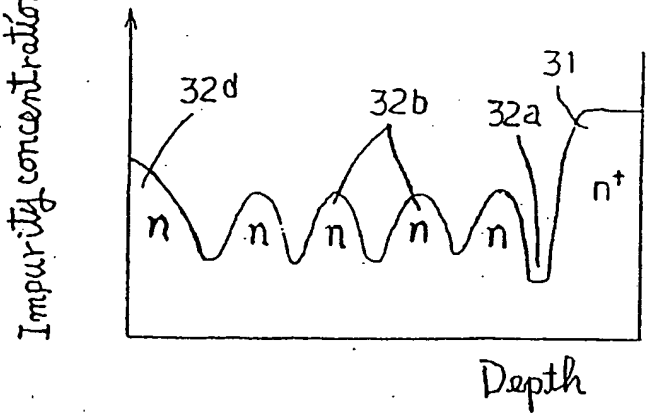


Fig.3(c)

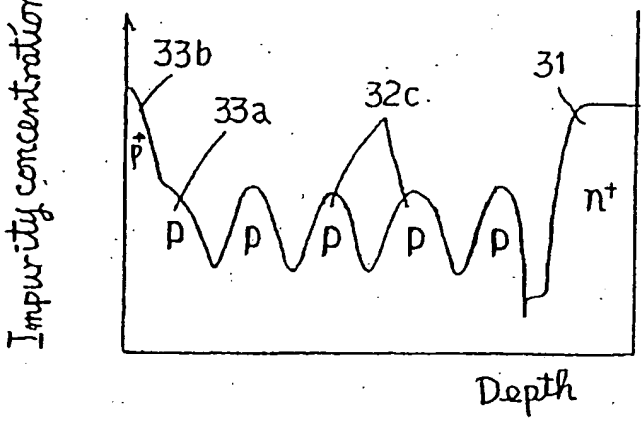


Fig.4(a)

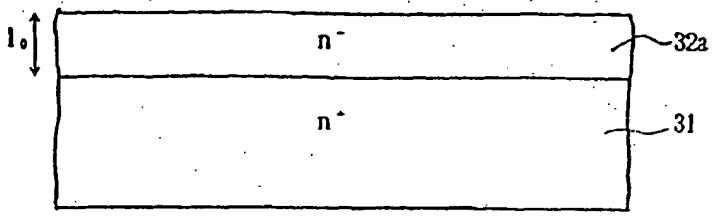


Fig.4(b)

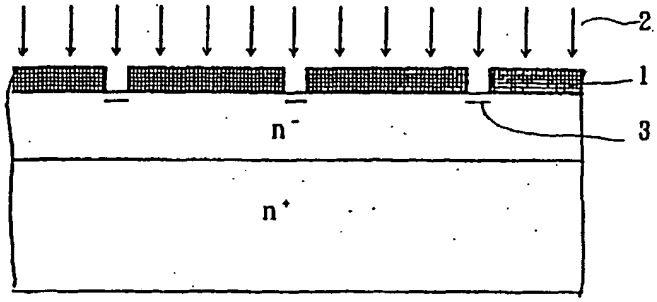


Fig.4(c)

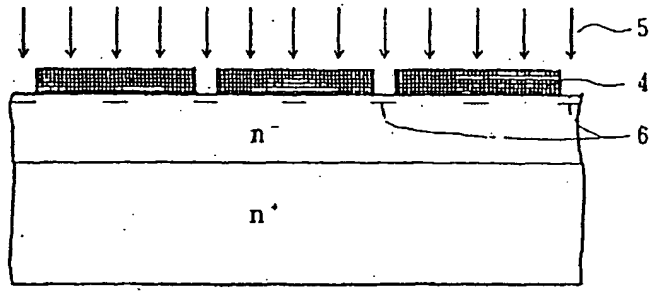


Fig.4(d)

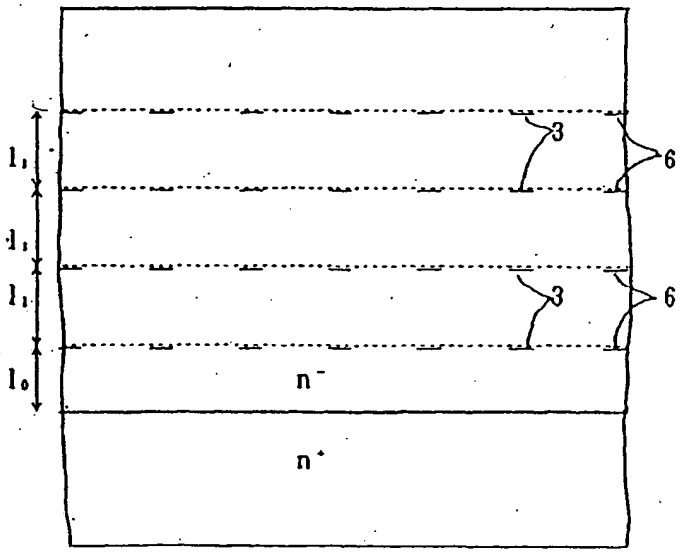


Fig. 5 (a)

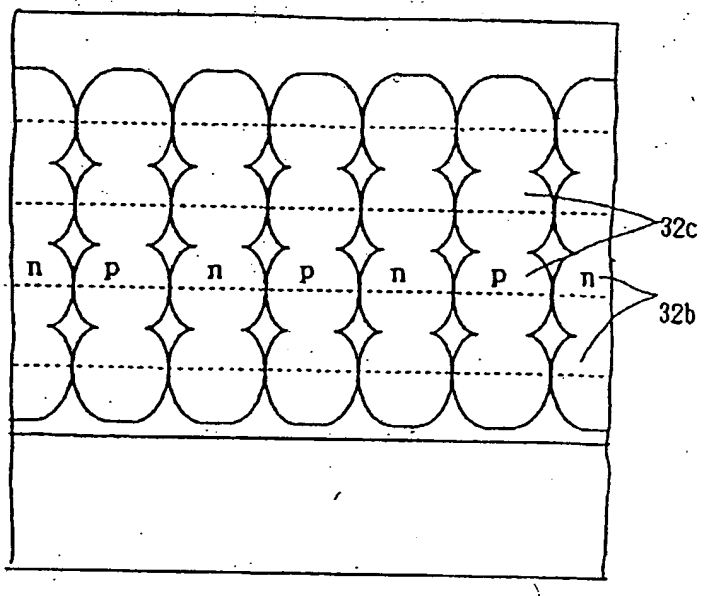


Fig. 5 (b)

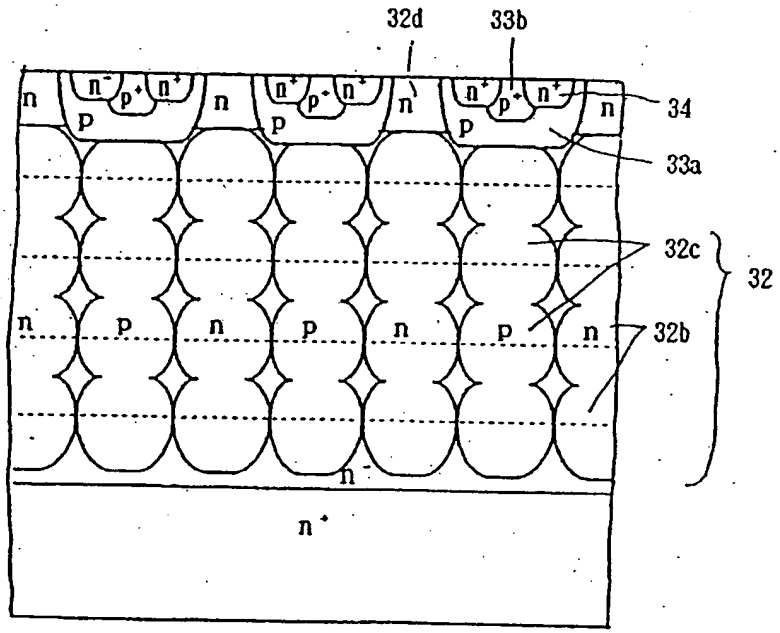


Fig. 6

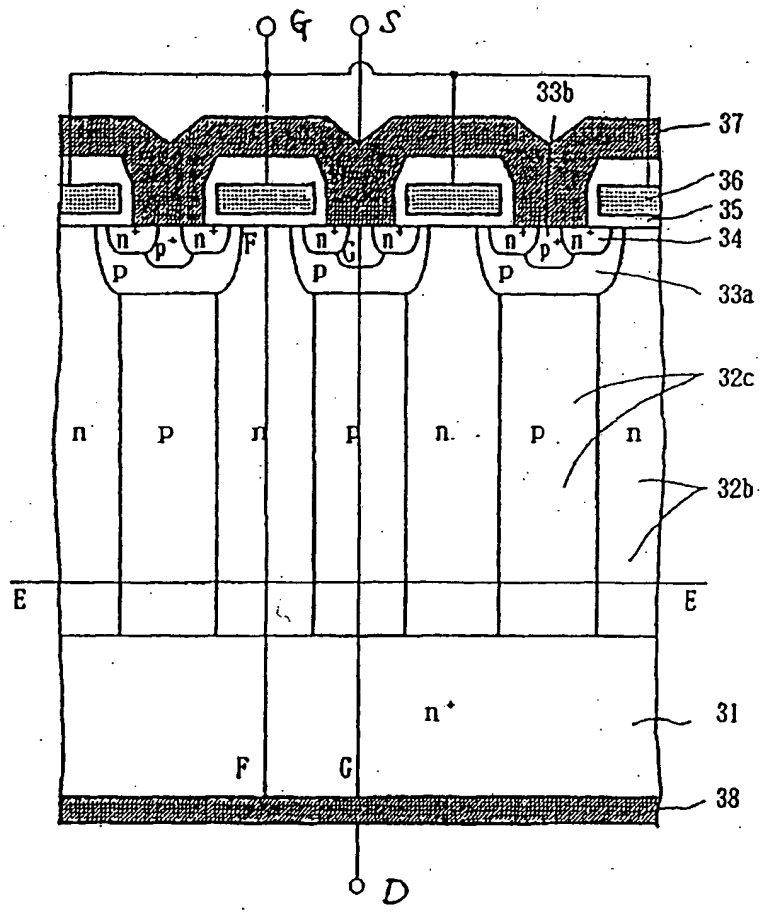


Fig.7

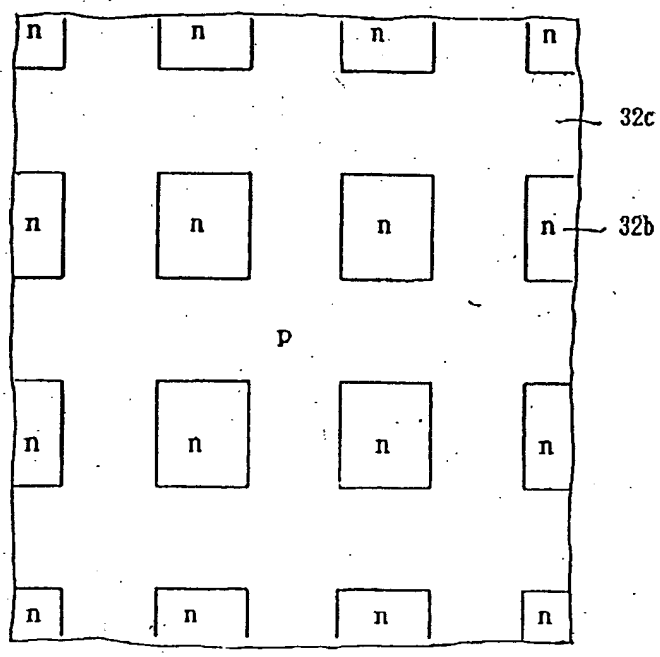


Fig.8

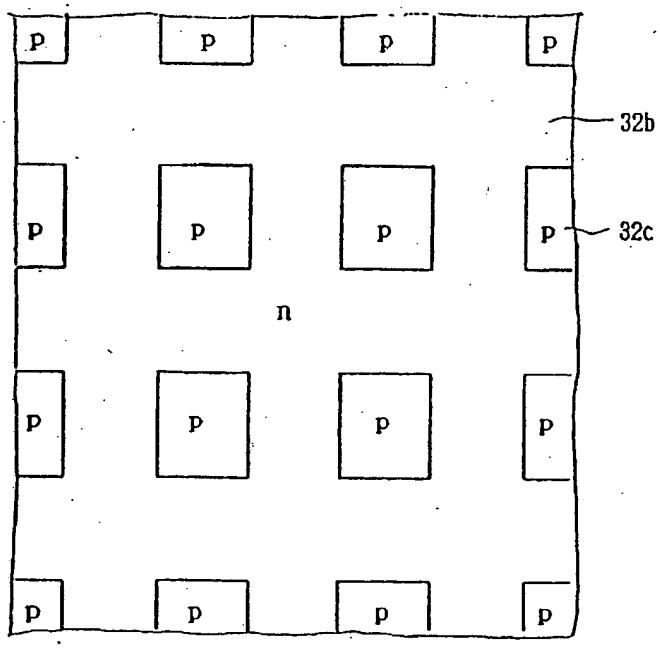


Fig. 9

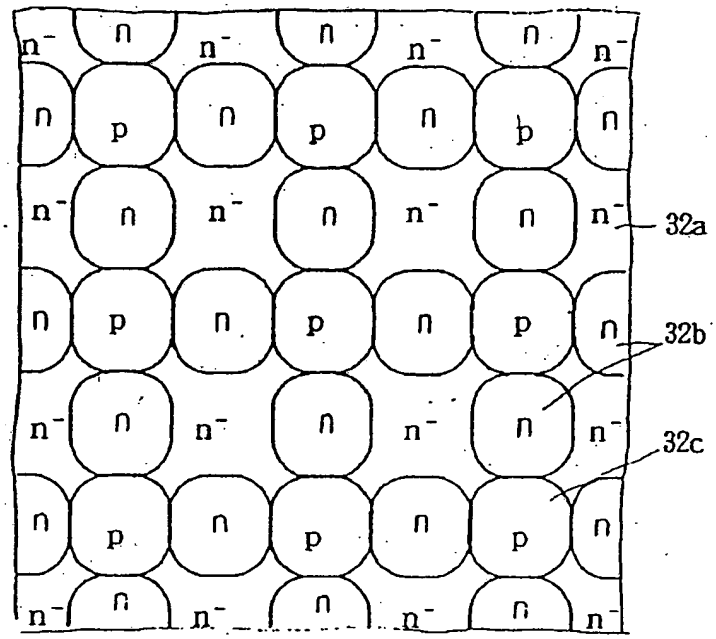


Fig. 10

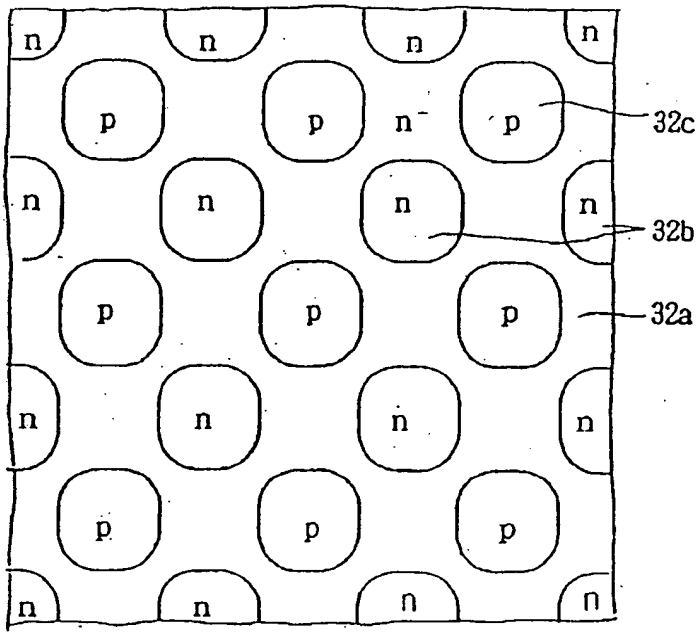


Fig.11

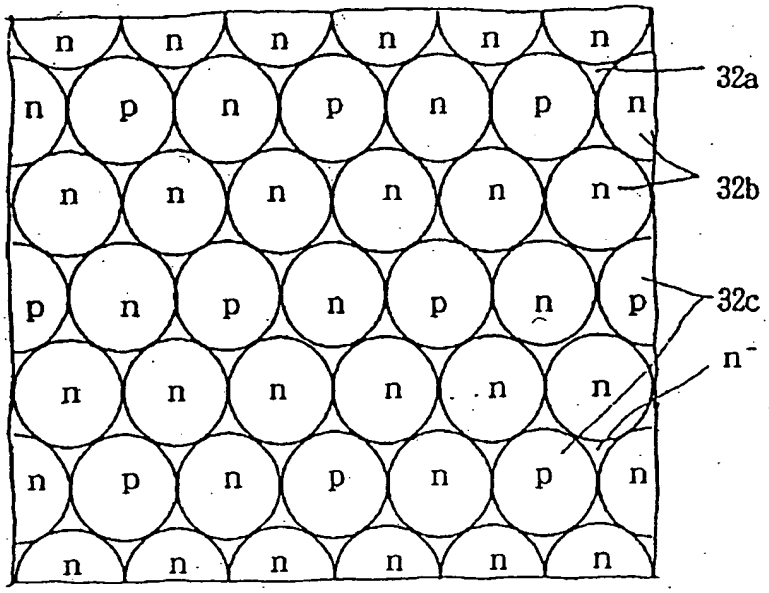


Fig.12

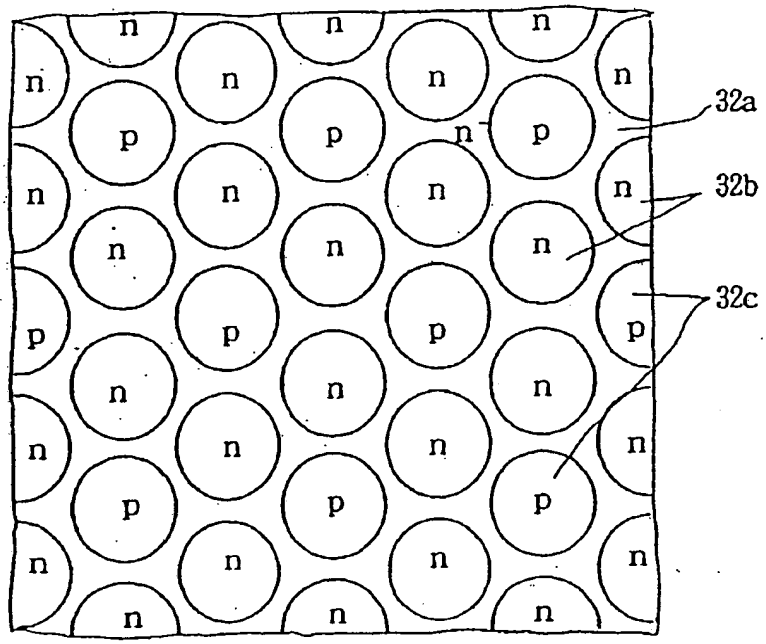


Fig.13

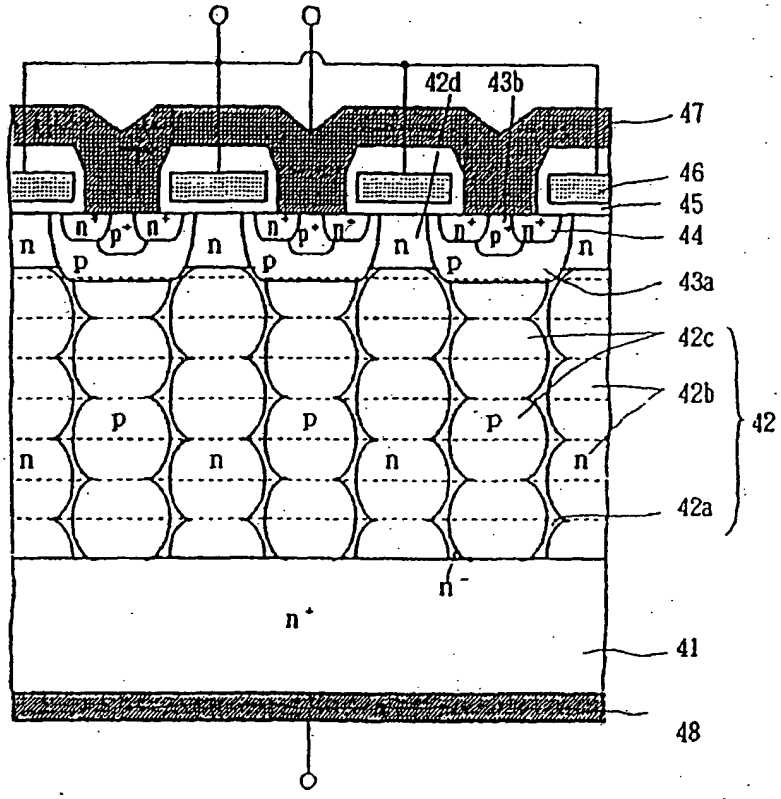


Fig.14

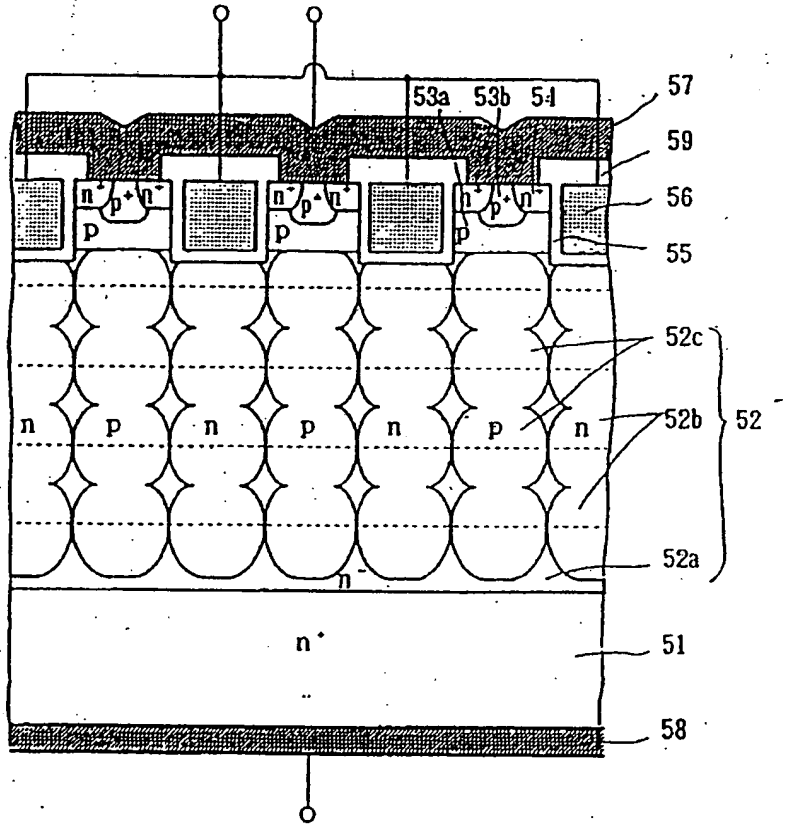
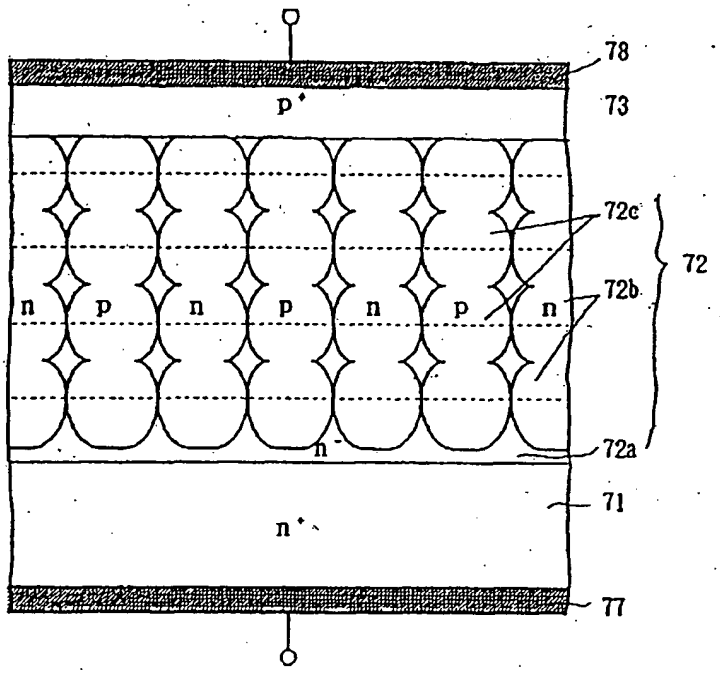


Fig.16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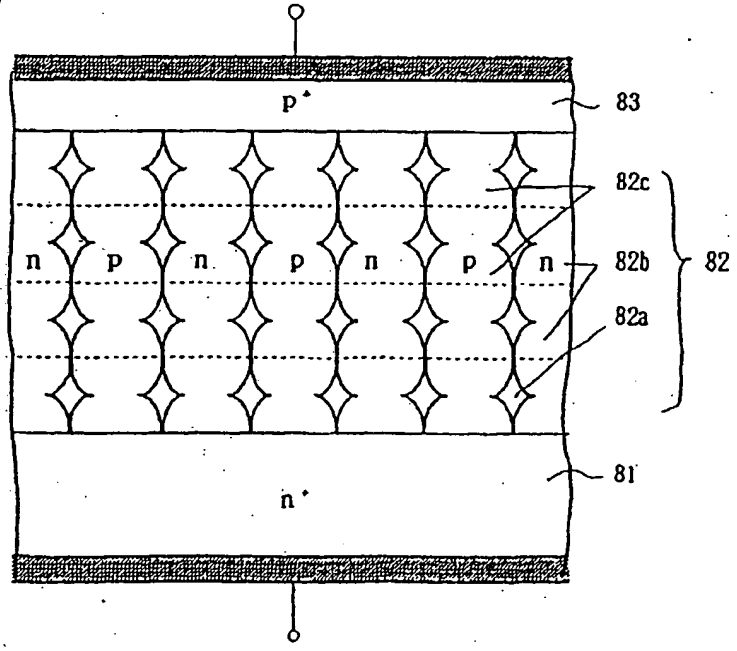
72c
72
n
p
n
p
n
p
n
72b
n-
72a
71
n+
77

Fig.17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82c
n
p
n
p
n
p
n
82b
82
82a
81
n+

Fig.18

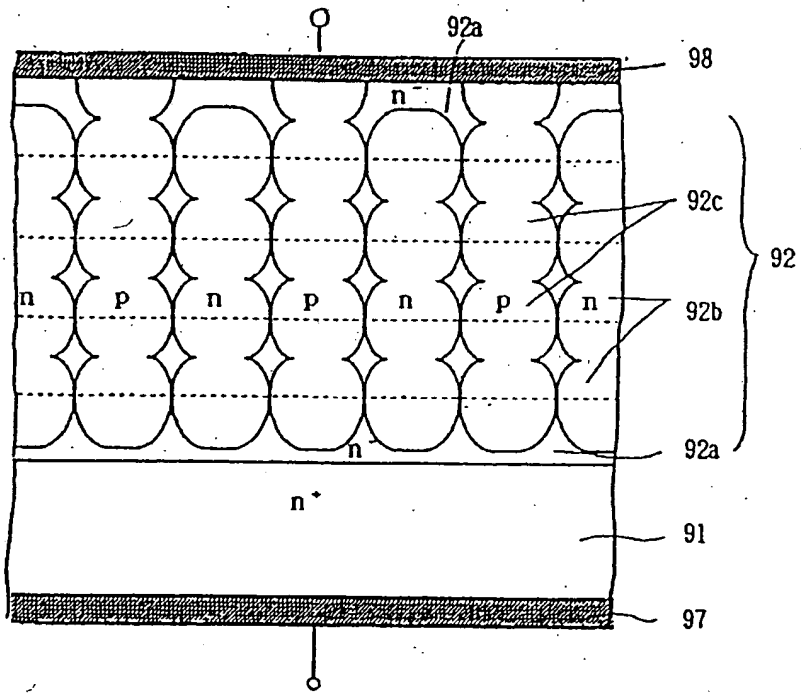


Fig.19

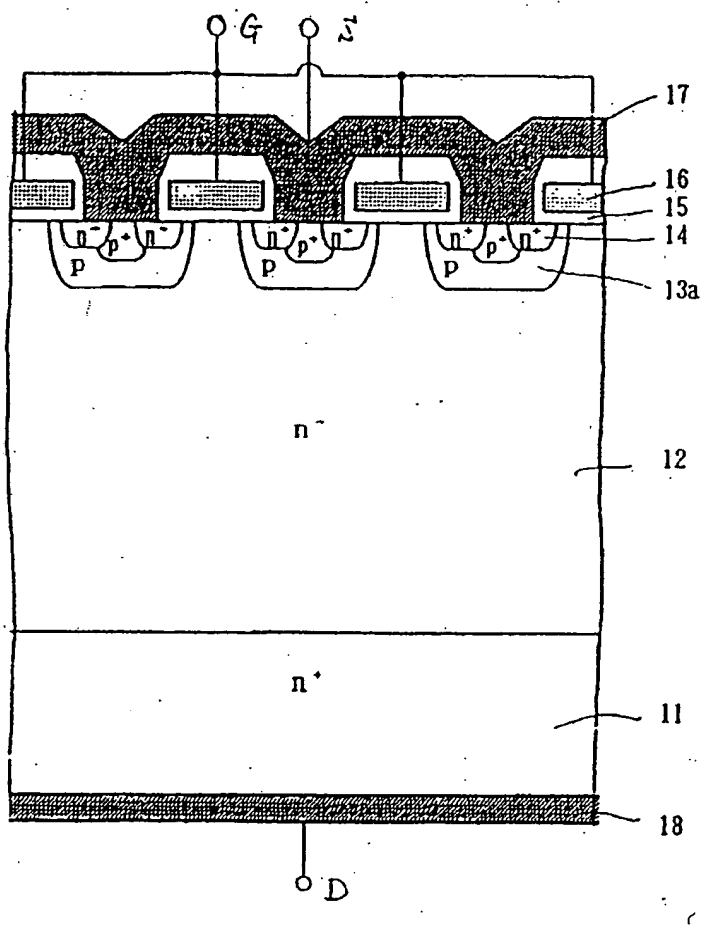
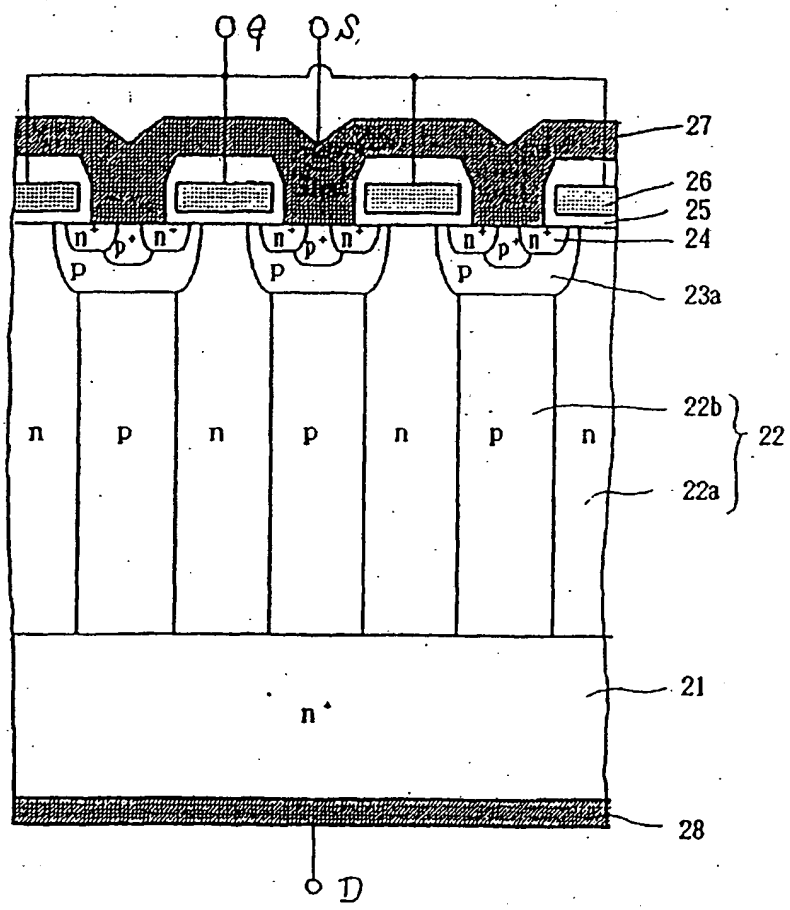


Fig.20



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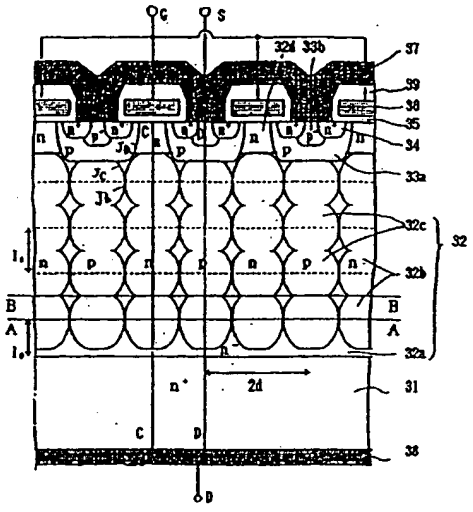
(54) Semiconductor device with alternating conductivity type layer and method of manufacturing the same

(57) The semiconductor device according to the invention includes a semiconductive substrate region 32, through that a current flows in the ON-state of the device and that is depleted in the OFF-state. The semiconductive substrate region 32 includes a plurality of vertical alignments of n-type buried regions 32b and a plurality of vertical alignments of p-type buried regions 32c. The vertically aligned n-type buried regions 32b and the vertically aligned p-type buried regions 32c are alternately arranged horizontally.

The n-type buried regions 32b and p-type buried regions 32c are formed by diffusing respective impurities into highly resistive n−-type layers 32a laminated one by one epitaxially.

Fig.1



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EUROPEAN SEARCH REPORT

Application Number
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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WO 97 29518 A (SIEMENS AG ET AL) 14 August 1997 (1997-08-14) * page 6, line 21 - page 9, line 28; figure 1 * * page 13, line 23 - page 14, line 24; figures 7A-7D *	1-22	H01L29/78 H01L29/739 H01L29/861 H01L29/872 H01L29/06 H01L29/36
D,A	US 5 438 215 A (TIHANYI J) 1 August 1995 (1995-08-01) * column 2, line 45 - line 62; figures 2-4 *	9-17	
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	17 October 2000	Morvan, D

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